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[54] FLATTENING METHOD AND FLATTENING APPARATUS OF A SEMICONDUCTOR DEVICE

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451/444, 72, 561

[56] References Cited

U.S. PATENT DOCUMENTS

3,568,377	3/1971	Blohm et al.	451/444
3,594,963	7/1971	Beasley	451/42
3,710,517	1/1973	Valerio et al.	451/42
3,785,094	1/1974	Holzhauser	451/532
5,154,021	10/1992	Bombadier et al.	451/444
5,172,681	12/1992	Ruark et al.	451/443
5,235,959	8/1993	Frank et al.	451/443

FOREIGN PATENT DOCUMENTS

4-35870 2/1992 Japan 451/444

OTHER PUBLICATIONS

Semiconductor International, Mar. 1992, pp. 44-48, Peter H. Singer, Senior Editor.

Spin-On Glass for Dielectric Planarization By Satish K. Gupta Distributed through the courtesy of Allied-Signal Inc., Milpitas, CA.

Solid State Technology May 1992, Sematech Inc., Austin, Texas Planarizing Interlevel Dielectrics by Chemical-Mechanical Polishing.

Electronics Materials, Mar. 1994, pp. 91-96.

Speedfam CMP-V Planarization System, The Competitive Edge. 0.35, Micron Line Width Design Rule.

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[57] ABSTRACT

A method for flattening an inter-layer insulating film of a semiconductor device of a multi-wiring is carried out with a chemical-mechanical polishing process by using an apparatus, which includes two-layer polishing cloth having an unwoven cloth and a hard foamed layer affixed on a support plate. In order to fluff on a surface of the hard foamed layer or recreate on the whole surface thereof, a tool is provided on the polishing cloth. A silicon wafer is held through a backing pad so that an insulating film of a semiconductor device formed on the wafer is polished by the polishing cloth by rotation of the support plate and the wafer, and at the same time the surface layer of the polishing cloth is fluffed by the tool provided with a polishing surface having the curvature as that of the backing pad. Therefore, a polishing rate can be kept stable, and uniformity of polishing quantity is improved.

21 Claims, 12 Drawing Sheets

